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Attorneys for Defendant
D-LINK SYSTEMS, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

3COM CORPORATION,

Plaintiff,

v.

D-LINK SYSTEMS INC.,

Defendant.

No. C-03-2177 VRW

JOINT CLAIM CONSTRUCTION AND PREHEARING STATEMENT PURSUANT TO PATENT L.R. 4-3

Under Patent L.R. 4-3, Plaintiff, 3Com, and Defendant, D-Link, propose construing the terms and claim elements identified below as follows.

The parties exchanged proposed terms and claim elements for construction pursuant to Patent L.R. 4-1. The parties thereafter exchanged proposed constructions for each term and claim element pursuant to Patent L.R. 4-2 and conducted a meet-and-confer conference regarding the proposed terms and claim elements. The parties expressly reserve their rights to propose constructions of additional terms, phrases or clauses in the asserted patents at a later time. In addition, the parties expressly reserve their rights to supplement or amend the proposed construction and other positions set forth herein.

I.

CLAIM TERMS, PHRASES, OR CLAUSES ON WHICH THE PARTIES AGREE.

Pursuant to Patent L.R. 4-3(a), the parties identify those claims terms, phrases, or clauses on which the parties agree:

Claim Term	Joint Construction
task	A processing routine.
network interface adapter	Equipment between a host computer and a communications medium for enabling communication.
in parallel	A period of concurrent operation.
monitoring	Watching, keeping track of, or checking on.
threshold determination	A determination of whether the threshold amount has been reached.
bad frame signal	A specific signal flag indicating that a corresponding frame contains invalid data.
threshold logic	Circuitry or a device for making a threshold determination.
host computer / host system	A computer that communicates over a network.
network	A system of computers, terminals, and databases connected by communications paths.

Claim Term	Joint Construction
CSMA/CD	A carrier sense multiple access (CSMA) with collision detection (CD) network, such as an Ethernet network.
communications medium	A network path through which frames are transmitted or received.
underrun condition	The condition of falling behind. See construction for "falls behind."
indication signal	A signal that is used to point out or to notify.
medium access controller	Circuitry or a device that controls access to the network.
optimizing the threshold value/ optimizing the threshold amount	Adjusting the current threshold amount to make it as perfect, effective, or functional as possible.

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II.

PARTIES PROPOSED CONSTRUCTION OF CLAIM TERMS, PHRASES, OR CLAUSES ON WHICH THE PARTIES DO NOT AGREE.

Pursuant to Patent L.R. 4-3(b), the parties identify the following claims terms, phrases, or clauses on which the parties disagree for construction by the Court:

A. Claim Terms Not Asserted By Parties As Subject To Construction According To §112, 6th Paragraph.

Claim Term	3Com's Proposed Construction	D-Link's Proposed Construction
buffer memory	Intermediate storage to facilitate the timely and ordered transfer of data between a host computer and a communications medium, including retaining the data for retransmission	Dedicated random access memory that (1) stores transmit data, (2) is distinct from a FIFO, (3) can always retransmit a frame of data without having to retrieve it from a host, and (4) controlled independently of the host system.

Claim Term	3Com's Proposed Construction	D-Link's Proposed Construction
Feedback	Current condition information available for control	Information derived from an output used to adjust an input.
Altering the threshold value	Changing the threshold value	Dynamically changing a threshold value by the host.
host system alterable threshold store	A place for storing a host computer changeable threshold amount	A storage location capable of change by the host dynamically.
alterable storage location	A place for storing changeable information	A storage location capable of change by the host dynamically.
posting status information	Storing the current condition information	Storing information about the state of a function or operation.
frame	Data bracketed by and including opening and closing sequences, such as a packet, for communication over a network.	A group of data transmitted as a unit that carries a protocol data unit on a network.
threshold amount/ threshold value	A value representing the quantity of data of a frame sufficient to trigger the initiation of transmission	A set value indicating a desired limit.
falls behind	When the frame is transmitted to the communications medium and some data from the host computer is not received in time to be included in the frame.	The absence of a write signal during a specified interval.

3Com's identification of references from the specification or prosecution history that support its constructions, and identification of extrinsic evidence known to 3Com on which it intends to rely either to support its proposed construction or to oppose D-Link's proposed constructions, is set out in Exhibit "A."

D-Link's identification of references from the specification or prosecution history that support its constructions, and identification of extrinsic evidence known to D-Link on which it intends to rely either to support its proposed construction or to oppose 3Com's proposed constructions, is set out in Exhibit "B."

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B. Claim Terms In Dispute Where The Parties Also Dispute Whether §112, 6th Paragraph Applies.

Claim Term	3Com's Proposed Construction And Supporting Evidence	D-Link's Proposed Construction And Supporting Evidence
transmit logic, responsive to the means for initiating transmission, for retrieving data from the buffer memory and supplying retrieved data for transmission on the communications medium	35 U.S.C. §112, ¶6 does not apply. This element should be construed according to ordinary principles of claim construction. The transmit logic is circuitry or a device that performs the recited functions. Corresponding structure if §112, ¶6 is found to apply: A disclosed structure in the '872 patent includes the interface controller 6 (*see* '872, col. 4:7-17), transmit DMA module 67, (*see* '872, col. 9:5-7; 13-18), the transmit logic 39 (*see* '872, col. 4:34-40), interface processor 14 (*see* '872, col. 5:36-48), transmit DMA logic 109 and transmit DMA 155.	D-Link asserts that 35 U.S.C. §112, ¶6, applies to this term. If 35 U.S.C. §112, ¶6, does not apply, D-Link's proposed construction is as follows: Circuitry or a device for retrieving data from a buffer memory for transmission over a communications medium. If 35 U.S.C. §112, ¶6, does apply, D-Link's proposed structure as corresponding to this term is as follows: Transmit MAC logic 39 in Fig. 2; network interface processor 14 in Fig. 3; elements 50, 66 and 67 in Fig. 4 and 4A; Xmit DMA logic 109 in Fig. 5; transmit DMA logic 155 in Fig. 9; elements 320 and 321 in Fig. 12; elements 330, 331, and 332 in Fig. 13; elements 335, 336, and 337 in Fig. 14; elements 340, 341, and 342 in Fig. 15, elements 350, 351, 353, 353, 354, 355, 356, and 357 in Fig. 16, and elements 400, 405, 407, 410, 411, and 413 in Fig. 18.
means, coupled with the buffer memory, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory	35 U.S.C. §112, ¶6 does not apply. This element should be construed according to ordinary principles of claim construction. The means is circuitry or a device coupled with the buffer memory that performs the recited functions. Corresponding structure if §112, ¶6 is found to apply: A disclosed structure in the '872	D-Link asserts that 35 U.S.C. §112, ¶6, applies to this term. If 35 U.S.C. §112, ¶6, does not apply, D-Link's proposed construction is as follows: Circuitry or a device, connected to a buffer memory, for watching, keeping track of, or checking on, the amount of data sent from a host computer to the buffer memory to determine whether the amount

Claim Term	3Com's Proposed Construction And Supporting Evidence	D-Link's Proposed Construction And Supporting Evidence
	patent includes the interface controller 6 (*see* '872, col. 4:7-17), early transmit logic 6A (*see* '872, col. 4:7-17), threshold logic 36 (*see* '872, col. 4:34-40), download DMA module 58 (*see* '872, col. 8:55-59; col. 9:5-7), interface processor 14 (*see* '872, col. 5:36-48), Fig. 11, 12, 13, 14, 15, 16 and 17.	of sent data has reached a set value indicating a desired limit. If 35 U.S.C. §112, ¶6, does apply, D-Link's proposed structure as corresponding to this term is as follows: Early transmit logic 6A in Fig. 1; threshold logic 36 in Fig. 2; network interface processor 14 in Fig. 3; download DMA 58 in Figs. 4 and 4A; elements 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 320, 321, 322, 323 in Figs. 11 and 12; elements 330, 331, and 332 in Fig. 13; elements 335, 336, and 337 in Fig. 14; elements 340, 341, and 342 of Fig. 15; elements 350, 351, 352, 353, 354, 355, 356, 357 in Fig. 16; and elements 370, 371, 372, and 373 in Fig. 17.
logic, coupled to the buffer memory, which monitors the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory	35 U.S.C. §112, ¶6 does not apply. This element should be construed according to ordinary principles of claim construction. The logic is circuitry or a device coupled to the buffer memory that performs the recited functions. Corresponding structure if §112, ¶6 is found to apply: A disclosed structure in the '872 patent includes the interface controller 6 (*see* '872, col. 4:7-17), early transmit logic 6A (*see* '872, col. 4:7-17), threshold logic 36 (*see* '872, col. 4:34-40), download DMA module 58 (*see* '872, col. 8:55-59; col. 9:5-7), interface processor 14 (*see* '872, col. 5:36-48), Figs. 11, 12, 13, 14, 15, 16 and 17.	D-Link asserts that 35 U.S.C. §112, ¶6, applies to this term. If 35 U.S.C. §112, ¶6, does not apply, D-Link's proposed construction is as follows: Circuitry or a device, connected to a buffer memory, for watching, keeping track of, or checking on, the amount of data sent from a host computer to the buffer memory to determine whether the amount of sent data has reached a set value indicating a desired limit. If 35 U.S.C. §112, ¶6, does apply, D-Link's proposed structure as corresponding to this term is as follows: Early transmit logic 6A in Fig. 1; threshold logic 36 in Fig. 2; network interface processor 14 in Fig. 3; download DMA 58 in Figs. 4 and 4A; elements 300,

Claim Term	3Com's Proposed Construction And Supporting Evidence	D-Link's Proposed Construction And Supporting Evidence
		301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 320, 321, 322, 323 in Figs. 11 and 12; elements 330, 331, and 332 of Fig. 13; elements 335, 336, and 337 of Fig. 14; elements 340, 341, and 342 of Fig. 15; elements 350, 351, 352, 353, 354, 355, 356, 357 in Fig. 16; and elements 370, 371, 372, and 373 in Fig. 17.
means, coupled with the buffer memory and including a host system alterable threshold store for storing a threshold value, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory	35 U.S.C. §112, ¶6 does not apply. This element should be construed according to ordinary principles of claim construction. The means is circuitry or a device coupled with the buffer memory and includes a host system alterable threshold store that performs the recited functions. Corresponding structure if §112, ¶6 is found to apply: A disclosed structure in the '872 patent includes the threshold logic 36 (*see* '872, col. 4:34-40), interface processor 14 (*see* '872, col. 5:36-48), controller 6, download DMA 58 and Figs. 11 and 13-17	D-Link asserts that 35 U.S.C. §112, ¶6, applies to this term. If 35 U.S.C. §112, ¶6, does not apply, D-Link's proposed construction is as follows: Circuitry or a device, connected to a buffer memory, for watching, keeping track of, or checking on, the amount of data sent from a host computer to the buffer memory to determine whether the amount of sent data has reached a set value indicating a desired limit, wherein the circuitry or device includes a storage location capable of change by the host that stores the set value. If 35 U.S.C. §112, ¶6, does apply, D-Link's proposed structure as corresponding to this term is as follows: Early transmit logic 6A in Fig. 1; threshold logic 36 in Fig. 2; network interface processor 14 in Fig. 3; download DMA 58 in Figs. 4 and 4A; elements 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 320, 321, 322, 323 in Figs. 11 and 12; elements 330, 331, and 332 of Fig. 13; elements 335, 336, and 337 of Fig. 14; elements 340, 341, and 342 of Fig. 15; elements 350, 351, 352, 353, 354, 355, 356, 357 in Fig. 16;

Claim Term	3Com's Proposed Construction And Supporting Evidence	D-Link's Proposed Construction And Supporting Evidence
		and elements 370, 371, 372, and 373 in Fig. 17.
data transfer circuitry, having a host system interface, for transferring data of frames to the buffer memory	35 U.S.C. §112, ¶6 does not apply. This element should be construed according to ordinary principles of claim construction. The data transfer circuitry is circuitry that includes a host system interface that performs the recited functions. Corresponding structure if §112, ¶6 is found to apply: A disclosed structure in the '872 patent includes the interface controller 6 (*see* '872, col. 4:7-17), download DMA module 58 (*see* '872, col. 8:55-59; col. 9:5-7), host interface logic 31 (*see* '872, col. 4:56-60), interface processor 14 (*see* '872, col. 5:36-48), host interface logic 102 (*see* '872, col. 11:43-col. 12:22), download DMA logic 107 (*see* '872, col. 11:43-col. 12:22), receive DMA logic 110 (*see* '872, col. 11:43-col. 12:22), and download DMA logic 151 (*see* '872, col. 16:24-35), and elements 50, 51, 53, 54, 55 and 150.	D-Link asserts that 35 U.S.C. §112, ¶6, applies to this term. If 35 U.S.C. §112, ¶6, does not apply, D-Link's proposed construction is as follows: Circuitry or a device, having an interface to a computer that communicates over a network, for sending frame data to a buffer memory. If 35 U.S.C. §112, ¶6, does apply, D-Link's proposed structure as corresponding to this term is as follows: Host interface logic 31 in Fig. 2; network interface processor 14 in Fig. 3 (and specifically elements 50, 51, 53, 55, and 58 in Figs. 4 and 4A); host interface logic 102, and Xmit descriptor and download DMA logic 107 in Fig. 5; and host descriptor logic 150 and download DMA logic 151 in Fig. 9.
host interface means, having an interface to the host system, for transferring data between the host system and the buffer memory	35 U.S.C. §112, ¶6 does not apply. This element should be construed according to ordinary principles of claim construction. The host interface means is circuitry or a device that includes an interface to the host system that performs the recited functions. Corresponding structure if §112, ¶6 is found to apply: A disclosed structure in the '872 patent includes the interface controller 6 (*see* '872, col. 4:7-	D-Link asserts that 35 U.S.C. §112, ¶6, applies to this term. If 35 U.S.C. §112, ¶6, does not apply, D-Link's proposed construction is as follows: Circuitry or a device, including an interface to a computer connected to a network, for sending data between the computer and a buffer memory. If 35 U.S.C. §112, ¶6, does apply, D-Link's proposed structure as corresponding to this term is as follows:

Claim Term	3Com's Proposed Construction And Supporting Evidence	D-Link's Proposed Construction And Supporting Evidence
	17), download DMA module 58 (*see* '872, col. 8:55-59; col. 9:5-7), host interface logic 31 (*see* '872, col. 4:56-60), interface processor 14 (*see* '872, col. 5:36-48), host interface logic 102 (*see* '872, col. 11:43-col. 12:22), download DMA logic 107 (*see* '872, col. 11:43-col. 12:22), and download DMA logic 151 (*see* '872, col. 16:24-35) and elements 50, 51, 53, 54, 55, 57 and 150.	Host interface logic 31 in Fig. 2; network interface processor 14 in Fig. 3 (and specifically elements 50, 51, 53, 55, 57, and 58 in Figs. 4 and 4A); host interface logic 102 (including Xmit descriptor and download DMA logic 107 and View, Xfer, and Upload DMA logic 108) in Fig. 5; host descriptor logic 150 and download DMA logic 151 in Fig. 9.
network interface means, having an interface to the network transceiver and responsive to the means for initiating, for transferring data between the buffer memory and the network transceiver for transmission	35 U.S.C. §112, ¶6 does not apply. This element should be construed according to ordinary principles of claim construction. The network interface means is circuitry or a device that includes an interface to the network that performs the recited functions. Corresponding structure if §112, ¶6 is found to apply: A disclosed structure in the '872 patent includes the interface controller 6 (*see* '872, col. 4:7-17), transmit DMA module 67, (*see* '872, col. 9:5-7; 13-18), and interface processor 14 (*see* '872, col. 5:36-48).	D-Link asserts that 35 U.S.C. §112, ¶6, applies to this term. If 35 U.S.C. §112, ¶6, does not apply, D-Link's proposed construction is as follows: Circuitry or a device, including an interface to a network and responsive to the means for initiating, for sending data between a buffer memory and the network interface for transmission over the network. If 35 U.S.C. §112, ¶6, does apply, D-Link's proposed structure as corresponding to this term is as follows: Transmit MAC logic 39 in Fig. 2; network interface processor 14 in Fig. 3, elements 50, 66 and 67 in Fig. 4 and 4A; Xmit DMA logic 109 in Fig. 5, transmit DMA logic 155 in Fig. 9, elements 320 and 321 in Fig. 12; elements 330, 331, and 332 in Fig. 13; elements 335, 336, and 337 in Fig. 14; elements 340, 341, and 342 in Fig. 15, elements 350, 351, 353, 353, 354, 355, 356, and 357 in Fig. 16, and elements 400, 405, 407, 410, 411, and 413 in Fig. 18.
means, having a host system interface, for	35 U.S.C. §112, ¶6 does not apply. This element should be	D-Link asserts that 35 U.S.C. §112, ¶6, applies to this term.

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Claim Term	3Com's Proposed Construction And Supporting Evidence	D-Link's Proposed Construction And Supporting Evidence
transferring data of frames to the buffer memory	construed according to ordinary principles of claim construction. The means is circuitry or a device that includes a host system interface, that performs the recited functions. Corresponding structure if §112, ¶6 is found to apply: A disclosed structure in the '872 patent includes the interface controller 6 (*see* '872, col. 4:7-17), download DMA module 58 (*see* '872, col. 8:55-59; col. 9:5-7), host interface logic 31 (*see* '872, col. 4:56-60), interface processor 14 (*see* '872, col. 5:36-48), host interface logic 102 (*see* '872, col. 11:43-col. 12:22), download DMA logic 107 (*see* '872, col. 11:43-col. 12:22), download DMA logic 151 (*see* '872, col. 16:24-35) and elements 50, 51, 53, 54, 55 and 150.	If 35 U.S.C. §112, ¶6, does not apply, D-Link's proposed construction is as follows: Circuitry or a device, including an interface to a computer connected to a network, for sending frame data from the computer to a buffer memory. If 35 U.S.C. §112, ¶6, does apply, D-Link's proposed structure as corresponding to this term is as follows: Host interface logic 31 in Fig. 2; network interface processor 14 in Fig. 3; elements 50, 51, 53, 54, 55, and 58 in Figs. 4 and 4A; host interface logic 102 and Xmit descriptor and download DMA logic 107 in Fig. 5; and host descriptor logic 150 and download DMA logic 151 in Fig. 9.
underrun control logic, which detects a condition in which the means for transferring falls behind the transmit logic, and supplies a bad frame signal to the communications medium in response to the underrun condition	35 U.S.C. §112, ¶6 does not apply. This element should be construed according to ordinary principles of claim construction. The underrun control logic is circuitry or a device that performs the recited functions. Corresponding structure if §112, ¶6 is found to apply: A disclosed structure in the '872 patent includes the interface processor 14 (*see* '872, col. 5:36-48), transmit logic 39 (*see* '872, col. 4:34-40; col. 28:25-40), and underrun detector 413 (*see* '872 col. 28:48-61).	D-Link asserts that 35 U.S.C. §112, ¶6, applies to this term. If 35 U.S.C. §112, ¶6, does not apply, D-Link's proposed construction is as follows: Circuitry or a device that detects a condition in which there is an absence of a write signal during a specified interval, and, in response thereto, supplies to a communications medium a specific signal flag indicating that a corresponding frame contains invalid data. If 35 U.S.C. §112, ¶6, does apply, D-Link's proposed structure as corresponding to this term is as follows: Underrun detector 413, and

Claim Term	3Com's Proposed Construction And Supporting Evidence	D-Link's Proposed Construction And Supporting Evidence
		elements 405, 407, 410, and 411 in Fig. 18.
logic, responsive to the threshold determination of the logic which monitors the transferring of data to the buffer memory, which initiates transmission of the frame from the buffer memory to the medium access controller prior to transfer of all of the data of the frame to the buffer memory, including logic which initiates transmission of the frame when no complete frame of data is present in the buffer memory	35 U.S.C. §112, ¶6 does not apply. This element should be construed according to ordinary principles of claim construction. The logic is circuitry or a device that performs the recited functions. Corresponding structure if §112, ¶6 is found to apply: A disclosed structure in the '872 patent includes the transmit logic 39 (*see* '872, col. 4:34-40), download DMA module 58 (*see* '872, col. 8:55-59; col. 9:5-7), interface processor 14 (*see* '872, col. 5:36-48), Fig 12.	D-Link asserts that 35 U.S.C. §112, ¶6, applies to this term. If 35 U.S.C. §112, ¶6, does not apply, D-Link's proposed construction is as follows: Circuitry or a device, responsive to a determination of whether a threshold amount has been reached by the logic which monitors the transferring of data to the buffer memory, which starts transmitting a frame from the buffer memory to circuitry or a device that controls access to the network before the buffer memory has received the whole frame, including circuitry or a device which starts transmitting a frame when an entire is not stored in the buffer memory. If 35 U.S.C. §112, ¶6, does apply, D-Link's proposed structure as corresponding to this term is as follows: Transmit MAC logic 39 in Fig. 2; network interface processor 14 in Fig. 3; download DMA 58 in Figs. 4 and 4A; elements 320, 321, 322, and 323 in Fig. 12; elements 330, 331, and 332 in Fig. 13; elements 335, 336, and 337 of Fig. 14; elements 340, 341, and 342 of Fig. 15; elements 370, 371, 372, and 373 of Fig. 17; and elements 400, 405, 407, 410, 411, and 413 in Fig. 18.
means for comparing the counter to the threshold value in the alterable storage location and generating an	35 U.S.C. §112, ¶6 does not apply. This element should be construed according to ordinary principles of claim construction. The means is circuitry or a	D-Link asserts that 35 U.S.C. §112, ¶6, applies to this term. If 35 U.S.C. §112, ¶6, does not apply, D-Link's proposed construction is as follows:

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Claim Term	3Com's Proposed Construction And Supporting Evidence	D-Link's Proposed Construction And Supporting Evidence
indication signal to the host processor responsive to a comparison of the counter and the alterable storage location.	device that performs the recited functions. Corresponding structure if §112, ¶6 is found to apply: A disclosed structure in the '459 patent includes the interface processor 14 (*see, e.g.*, '459, col. 7:8-9), DMA Block 63 (*see* '459, col. 11:20-41; col. 31:25-33), and threshold compare logic 511.	Circuitry or a device for comparing a count value to a set value indicating a desired limit that is stored in a location capable of change by the host dynamically, and, in response to the comparing the count value to the stored set value, generating a signal that is used to point out or to notify to the host processor. If 35 U.S.C. §112, ¶6, does apply, D-Link's proposed structure as corresponding to this term is as follows: Fig. 14, comparator 213 and RCV complete control 210.

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C. Claim Terms In Dispute Where The Parties Agree That §112, 6th Paragraph Applies.

Claim Term	3Com's Proposed Construction And Supporting Evidence	D-Link's Proposed Construction And Supporting Evidence
control means, coupled with the network interface means, for posting status information for use by the host system, as feedback for optimizing the threshold value	A disclosed structure in the '872 patent includes host interface logic 31 (*see* '872, col. 4:46-60) and interface processor 14 (*see* '872, col. 5:36-48).	Info and Status registers in Fig. 6; underrun detector 413 in Fig. 18.
means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame, prior to transfer of all the data of the frame to the buffer memory from	A disclosed structure in the '872 patent includes the interface controller 6 (See '872, col. 4:7-17), download DMA module 58, (*see* '872, col. 8:55-59; col. 9:5-18), interface processor 14 (*see* '872, col. 5:36-48) and transmit MAC logic 39.	Transmit MAC logic 39 of Fig. 2; network interface processor 14 in Fig. 3; download DMA 58 in Figs. 4 and 4A; elements 320, 321, 322, and 323 in Fig. 12; elements 330, 331, and 332 of Fig. 13; elements 335, 336, and 337 of Fig. 14; elements 340, 341, and 342 of Fig. 15; elements 370, 371, 372, and 373 of Fig. 17; and elements

Claim Term	3Com's Proposed Construction And Supporting Evidence	D-Link's Proposed Construction And Supporting Evidence
the host computer		400, 405, 407, 410, 411, and 413 in Fig. 18.

III.

ESTIMATED TIME FOR CLAIM CONSTRUCTION HEARING.

Under Patent L.R. 4-3(c), the parties anticipate the following length of time necessary for the Claim Construction Hearing: one day.

IV.

IDENTIFICATION OF WITNESSES.

As required by Patent L.R. 4-3(d), the parties identify the following witness each party may call at the Claim Construction Hearing:

3Com may present testimony at the claim construction hearing from an expert, Mr. Alfred C. Weaver. Pursuant to Patent L.R. 4-3(d), 3Com presents a summary of each opinion to be offered by its expert in Exhibit A.

D-Link may present testimony at the claim construction hearing from its expert, Mr. Howard Frazier. Pursuant to Patent L.R. 4-3(d), D-Link presents a summary of each opinion to be offered by its expert in Exhibit "C."

V.

OTHER ISSUES.

Under Patent L.R. 4-3(e), parties identify the following "other issues" to be addressed at the Claim Construction Hearing:

None at this time.

Pursuant to the Court's request, the parties are in the process of scheduling a new date for the claim construction hearing, due to the Court's unavailability on the date originally scheduled.

Respectfully,

DATED: March 12, 2004.

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By: /s/
NEIL A. SMITH

Attorneys for Plaintiff 3COM CORPORATION

DATED: March 12, 2004.

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By: /s/
STEVEN H. MORRISSETT

Attorneys for Defendant D-LINK SYSTEMS, INC.